

TITLE: MULTI-BANK MEMORY  
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SERIAL NO.: 09/809,586

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TP  
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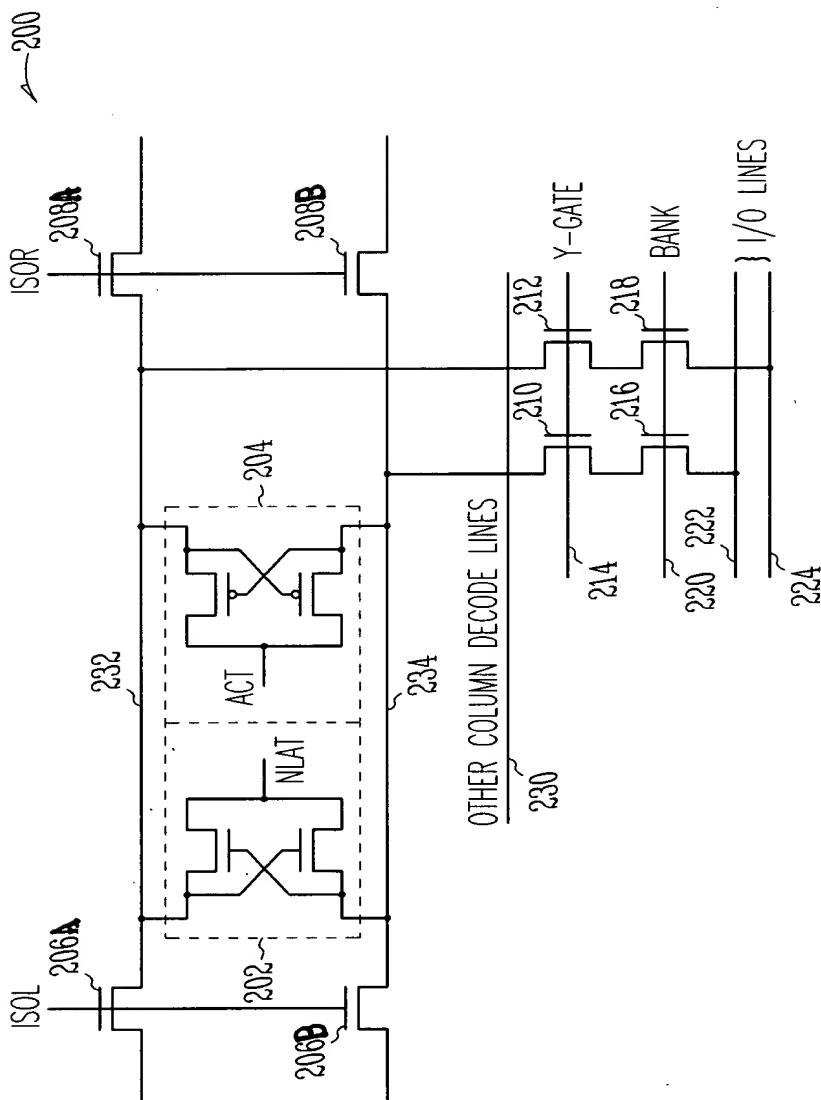


Fig. 2 (Prior Art)

The diagram illustrates a memory array structure. At the top, a horizontal line is labeled **ISOL**. Below it, two vertical lines are labeled **406A** and **406B**. A dashed box labeled **402** encloses two cross-coupled inverters. The left inverter is labeled **NI/AT** and the right inverter is labeled **ACT**. A dashed box labeled **404** encloses the right inverter. Below the inverters, a horizontal line is labeled **432**. At the bottom, a horizontal line is labeled **ISOL**. To the right of the array, a vertical line is labeled **408A** and **408B**. A dashed box labeled **434** encloses the right inverter. Below the array, a horizontal line is labeled **430** and is associated with the label **OTHER COLUMN DECODE LINES**. To the right of the array, a vertical line is labeled **414** and **412**. A dashed box labeled **422** encloses the right inverter. At the bottom right, a horizontal line is labeled **424** and is associated with the label **I/O LINES**.